REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 2, 3, 6-8, 10, 13, 14 , 19 and 20 are currently being cancelled.

Claims 1, 4, 5, 9, 12, 15-18 and 21 are currently being amended.

No claims are currently being added.

This amendment amends and cancels claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending and canceling the claims as set forth above, claims 1, 4, 5, 9, 11, 12, 15-18 and 21 are now pending in this application.

Claim Rejections – 35 U.S.C. § 101:

In the Office Action, claims 12-20 were rejected under 35 U.S.C. § 101 as being to non-statutory subject matter, for the reasons set forth on pages 5 and 6 of the Office Action. By way of this amendment and reply, independent claims 12, 15 and 17 have been amended to explicitly recite a step that provides a "useful, concrete and tangible" result (claims 13, 14, 16 and 18-20 have been canceled, thereby mooting the rejection of those claims). Also, claims 15-18 now recite a computer-readable medium embodying computer program product.

Accordingly, presently pending claims 12 and 15-18 are believed to fully comply with 35 U.S.C. § 101.

Claim Rejections – 35 U.S.C. § 112, 2nd Paragraph:

In the Office Action, claims 1-21 were rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite, for the reasons set forth on page 6 of the Office Action. This rejection is respectfully traversed. In particular, certain independent claims have been amended to recite additional features of the determining step, which can be found on page 27, 4-14 of the specification. This clearly describes how the "acceptability" criteria is made, and thus the issues raised on page 6 of the Office Action concerning this criteria have been addressed by way of these claim amendments. As to "intended use" features in the claims, Applicant respectfully disagrees, since the supposed "intended use" features are what is being performed

by the various steps/sections in the claims, and thus that does not correspond to intended use but rather explicit claim limitations that must be given patentable weight.

Accordingly, all of the presently pending claims are fully compliant with 35 U.S.C. § 112, 2nd Paragraph.

Claim Rejections – Prior Art:

In the Office Action, claims 1-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by "Applied Boolean Equivalence Verification and RTL Static Sign-Off", by Harry Foster; claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by "As good as gold", by Blackett; and claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by "On the Formal Verification of ATM Switches", by Jianping Lu. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

Turning now to the cited art of record, each of the presently pending independent claims (except some of the method claims that already recited certain features in an ending steps) recite a means for determining. For example, claim 1 recites means for determining, based on the logic cones, whether first logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits. Claim 1 also now includes the features of claim 2, now canceled, as well as other features added to that claim to more clearly distinguish over the cited art of record.

In more detail, presently pending independent claim 1 now recites:

based on the comparison of the first logic cones and the second logic cones, the determining means determines whether the RT level description that has been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits, and

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

No such comparing of first and second logic cones is performed in the system of Foster, so as to determine if an RT level description that has been designed in a behavioral

synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

On page 7 of Foster, which is cited against the features of claim 2, which are now incorporated into claim 1, it merely describes BDD-based techniques for providing equivalence between different functions, whereby there is no teaching or suggestion of determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits. Similarly, page 9 of Foster, which is also cited against the features of claim 2, which are now incorporated into claim 1, merely describes Equivalence checking with don't cares, whereby it does not teach or suggest determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Turning now to Blackett, the Office Action cites page 69, paragraph 1 and "A Practical Platform", paragraphs 3 and 4 of that reference, for allegedly teaching the features of claim 2, which have been incorporated into claim 1. Applicants respectfully disagree. Namely, page 69 of Blackett merely describes a form of logic representation that overcomes the limitations of BDDS, whereby that form of logic representation includes logic cones. This high-level description of the use of logic cones falls well short of teaching or suggesting a means for determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Lastly, turning now to Lu, the Office Action cites page 8, paragraph 3 of that reference, for allegedly teaching the features of claim 2, which have been incorporated into claim 1. Applicants respectfully disagree. Namely, page 8 of Lu merely describes algorithms in which the traversal of output logic cones is done such that the combinational inputs farthest from the outputs appear earlier in the ordering. This high-level description of the use of logic cones falls well short of teaching or suggesting a means for determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Put another way, it appears that the Office Action has found three references that describe the use of logic cones, and based on that alone, the Office Action asserts that those references teach or suggest the claimed invention. This is clearly not the case, since none of

those references teach the comparison of first and second logic cones to determine if they are logically equivalent, in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Accordingly, presently pending independent claim 1 is not anticipated by either Foster, Blackett or Lu.

Presently pending independent claims 5, 9, 12, 15 and 17 each recite features of determining whether first and second logic cones are logically equivalent, in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits, whereby those claims are not anticipated by either Foster, Blackett or Lu for reasons similar to those given above for claim 1.

Lastly, with respect to presently pending independent claim 21, that claim recites features seen best in Figure 4 of the drawings, whereby such features are not disclosed, taught or suggested by either Foster, Blackett or Lu. The Office Action appears to "punt" on its rejection of claim 21, by not providing any basis for the specific features in that claim, whereby the Office Action merely refers to the rejection of claims 1, 5 and 12. However, presently pending claim 21 recites structural features, such as first, second and third processing devices, and first, second and third storage sections, which do not appear in any of the other claims under rejection, whereby it is impossible to discern how the Examiner is using the rejections of claims 1, 5 and 12 for rejecting claim 21. Accordingly, since the Examiner has clearly not made out a prima facie case of anticipation with respect to claim 21, it is respectfully requested that the rejection of that claim be reconsidered and withdrawn.

To make these differences more clear, presently pending independent claim 21 has been amended so that all elements in that claim are now "means plus function" elements, whereby support for those elements can clearly be seen in Figure 4 of the drawings. Namely, storage device 1 on the left side of that figure corresponds to the claimed first storage means, storage device 1 that is the third-from-the-left in that figure corresponds to the claimed second storage means, and storage device 1 that is fifth-from-the-left in that figure corresponds to the claimed third storage means. The claimed determining means may correspond to element 3 in that figure. Similarly, the three data processing devices, from left to right in that figure, respectively correspond to the claimed first, second and third data processing means.

As one instance, the claimed third data processing means receives the behavioral level logic cones and the RT level logic cones stored in the third storage means, the correspondence information stored in the first storage means, and the compile information stored in the second storage means, and performs logic cone comparisons as a result thereof. The Office Action has not addressed any of these specific features in retrieving information stored in three separate storage means in order to perform logic cone comparisons, whereby such features are clearly not disclosed, taught or suggested by either Foster, Blackett or Lu. **Given that claim 21 is now recited as a means plus function claim in which the Examiner cannot assert that it recites "intended use statements", the Examiner must provide a detailed analysis of where each of these claim elements are found in the cited art of record, or otherwise withdrawn this rejection.**

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicant believes that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

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